REMARKS

Applicants have amended claim 30 to correct the spelling of "copper", in the last line of this claim. In view thereof, it is respectfully submitted that the objection to claim 30 as set forth in Item 2 on page 2 of the Office Action mailed March 18, 2002, is moot. It is respectfully requested that this Amendment of claim 30 be entered under 37 CFR 1.116(b), as complying with a requirement of form expressly set forth for the first time in the Office Action mailed March 18, 2002.

In any event, noting that the present amendment of claim 30 clearly overcomes the claim objection set forth in Item 2 on page 2 of the Office Action mailed March 18, 2002; that this amendment of claim 30 clearly does not raise any new issues, including any issue of new matter; and that this amendment of claim 30 satisfies a requirement by the Examiner made for the first time in the Office Action mailed March 18, 2002, entry of the present amendment of claim 30 is proper under 37 CFR 1.116(c).

In view of all of the foregoing, it is respectfully submitted that Applicants have made any necessary showing under 37 CFR 1.116; and that, accordingly, entry of the present amendment of claim 30 is clearly proper.

Applicants thank the Examiner for the indicated allowance of claims 1, 2, 4-6, 9-20, 22-25, 27-29, 31-35 and 37.

With respect to the rejected claims, claims 3, 30 and 36, it is respectfully submitted that the applied references, U.S. Patent No. 6,020,266 to Hussein, et al. and the article "Diffusion Barrier Between Copper and Silicon" in IBM Technical Disclosure Bulletin, vol. 35, no. 1B (June 1992), pages 214 and 215, would have neither taught nor would have suggested the subject matter of the claims rejected in

the Office Action mailed March 18, 2002.

Specifically, it is respectfully submitted that these references would have neither taught nor would have suggested such a semiconductor device with a multilayered structure as in the present claims, including the copper film interconnect having a neighboring film between a dielectric film of the multilayered structure and the copper film interconnect, the neighboring film being formed of ruthenium and being formed through sputtering, and the copper film interconnect having a multilayered structure including a copper film as formed through sputtering and a copper film as formed through plating or chemical vapor deposition. See claim 3.

Moreover, it is respectfully submitted that these applied references would have neither taught nor would have suggested such semiconductor device having a layered interconnection structure as in the present claims, with the layered interconnection structure including a copper film and a neighboring film adjacent to the copper film, and a dielectric film which is positioned such that the neighboring film is between the copper film and the dielectric film, the neighboring film containing a material selected from the group consisting of rhodium, ruthenium, iridium, osmium and platinum as the primary constituent element and being a film made by physical vapor deposition. See claim 30.

In addition, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested such a semiconductor device as in the present claims, having a layered interconnection structure which includes a copper film overlying the semiconductor substrate surface and a neighboring film, the device including a dielectric film overlying the semiconductor substrate surface, with the dielectric film positioned such that the

neighboring film is between the copper film and dielectric film, the neighboring film including a material selected from a group consisting of rhodium, ruthenium, iridium, osmium and platinum, and being made by physical vapor deposition. See claim 36.

That is, in connection with each of claims 3, 30 and 36, it is respectfully submitted that the combined teachings of these references would not have disclosed, nor would have suggested, the neighboring film between the copper film and the dielectric film, with the neighboring film made of the respective element (or selected from the group of elements) as in claims 3, 30 and 36, and with the copper film and/or the neighboring film made by physical vapor deposition (for example, sputtering).

The present invention is directed to a semiconductor device having a layered (for example, multilayered) interconnect structure. In recent large-scale-integrated semiconductor devices, copper interconnects are being employed since they have a lower electrical resistance than conventional aluminum interconnects. However, diffusion of copper in semiconductor devices into dielectric films thereof degrades characteristics of such devices; and, accordingly, diffusion barriers of, for example, titanium nitride, tungsten or tantalum have been used.

However, in large-scale-integrated semiconductor devices with fine patterns, in which high-density current occurs, electromigration (in which atoms are diffused into the dielectric layer owing to electron streams flowing in the fine patterns and due to heat generated by the flow of electrons) is a problem, causing voids and interconnect breakdowns. Use of a diffusion barrier of, e.g., titanium nitride, does not provide satisfactory electromigration resistance.

Against this background, Applicants have clarified a source of this diffusion problem, and having clarified such source, have found a technique which overcomes the problem. Applicants have clarified that, in a layered interconnect structure using, for example, a titanium nitride film as a diffusion barrier kept in contact with the copper film, the significant difference between the material of the diffusion barrier and copper in the length of the sides of the unit cell brings about a disordered atomic configuration at the interface therebetween, thereby promoting copper diffusion that results in problems of voids and interconnect breakdowns. Having clarified this problem, and in order to prevent the diffusion and, accordingly, the voids and breakdowns in copper interconnects, Applicants utilize materials that differ little from copper in a length of the sides of the unit cell. See the paragraph bridging pages 2 and 3 of Applicants' specification. Applicants have further found that where the difference between sides of the rectangular unit cells representing the copper and neighboring films is less than 13%, the aforementioned problems in voids and interconnect breakdowns are avoided.

In particular, Applicants have found specific materials for the neighboring film (adjacent the copper film), and also specific techniques for forming the various layers, whereby the aforementioned differential in lengths of sides of the units cells is sufficiently small, so as to avoid the diffusion, and resulting voids and interconnect breakdowns. That is, Applicants have found that by forming at least one of the adjacent layers of copper and neighboring film by physical vapor deposition, with selection of material of the neighboring film, the aforementioned problem of voids can be avoided, due to the structure formed.

Attention is respectfully directed to Figs. 2-5 of Applicants' original disclosure, together with the description on pages 13-16 of Applicants' specification. This shows that the diffusion coefficient of the copper film greatly increases in regions where there is a great size differential. It is respectfully submitted that this evidence in Applicants' specification must be considered in determining the question of unobviousness. See In re DeBlauwe, 222 USPQ 191 (CAFC 1984). It is respectfully submitted that this evidence shows unexpectedly lower diffusion occurs in connection with copper or platinum, on the one hand, and the various materials within the present claims, including ruthenium, on the other, where the difference in unit cell length is relatively small. This evidence shows unexpectedly better results achieved according to the present invention, and clearly establishes unobviousness of the present invention.

It is emphasized that in claims 3, 30 and 36, the neighboring film is provided interposed between the copper film (interconnect) and a dielectric film. It is respectfully submitted that a neighboring film between the copper and this dielectric film is different from, e.g., the use of barrier materials as disclosed in the IBM Technical Disclosure Bulletin article, preventing copper diffusion into silicon (a semiconductor). As will be shown in the following, it is respectfully submitted that the references as applied by the Examiner do not disclose, nor would have suggested, material including, for example, ruthenium, for use as a neighboring film between copper and a dielectric film, to avoid diffusion of copper into the dielectric film; and, accordingly, would have neither disclosed nor would have suggested the present invention.

Hussein, et al. discloses fabrication of via plugs and metal lines in interconnect systems, including use of a barrier layer formed onto a surface of a substrate that has at least one via, with a conductive layer formed on the barrier layer. A photoresist layer is formed on the conductive layer and patterned, with a metal via plug being formed onto the at least one via. A metal line is formed on the metal via plug, the layer of photoresist is removed, and the conductive layer not covered by the metal line is removed. See column 2, lines 14-22. This patent discloses use of appropriate conductive layers for the barrier layer 5, which may be titanium nitride or tantalum, and discloses barrier layer 5 is provided to prevent a metal line 11 that is later deposited in each via 4, from diffusing into the underlying and adjacent dielectric layer 3. Note column 1, lines 55-57; and column 3, lines 9-11, 18 and 19, and 55-58.

It is emphasized that Hussein, et al. discloses that barrier layer 5 is used to prevent diffusion of a metal line 11, later deposited, into the underlying and adjacent dielectric layer. Such disclosure as in Hussein, et al. would have neither disclosed nor would have suggested the presently claimed subject matter, including, in particular, wherein one of the specified materials for the neighboring film (e.g., ruthenium) as in claims 3, 30 and 36, is positioned between the dielectric film and the copper film interconnect.

It is respectfully submitted that the secondary reference as applied by the Examiner would not have rectified the deficiencies of Hussein, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

The IBM Technical Disclosure Bulletin article discloses a diffusion barrier between copper and silicon. This patent discloses that a metal ideally fulfilling criteria for such diffusion barrier between copper and silicon is rhenium, and that similar desirable values of elastic constant and eutectic temperature are a property of osmium, ruthenium and iridium as well.

It is respectfully noted that the IBM Technical Disclosure Bulletin article discloses a diffusion barrier between copper and silicon. In contrast, Hussein, et al. discloses a barrier layer between a metal line, e.g., of copper and an underlying and adjacent dielectric layer. It is respectfully submitted that one of ordinary skill in the art concerned with in Hussein, et al., looking to avoid diffusion of, e.g., copper into a dielectric layer, would not have looked to the teachings of the IBM Technical Disclosure Bulletin article, having a diffusion barrier between copper and silicon.

In this regard, it is respectfully submitted that the Examiner has pointed to no proper motivation for using the teachings of the IBM Technical Disclosure Bulletin article, of a diffusion barrier between copper and silicon, as a barrier layer in Hussein, et al. between copper and a dielectric layer. It is respectfully submitted that, from the teachings of the prior art references, one would not have known (for example, one would have not have had any predictable degree of success) as to whether a barrier material to prevent diffusion into silicon would have a same effect for preventing diffusion into another film (e.g., a dielectric film). Thus, it is respectfully submitted that it is improper to combine the teachings of Hussein, et al and the IBM Technical Disclosure Bulletin article as applied by the Examiner, under the guidelines of 35 USC 103; and that, in any event, the combined teachings of the applied references would have neither disclosed nor would have suggested the

neighboring film of, e.g., ruthenium, between the copper film interconnect and dielectric film, as in the present claims, since the IBM Technical Disclosure Bulletin article only describes, e.g., rhenium as a diffusion barrier between copper and silicon.

The contention by the Examiner that Hussein, et al. recognizes that copper diffusion into silicon and, also, into any surrounding dielectric material, can result in defective circuitry, is respectfully traversed. It is respectfully submitted that Hussein, et al., at column 1, lines 55-57, describes copper diffusion into a dielectric layer, not into silicon. Hussein, et al expressly and specifically discloses that the barrier layer prevents a metal line that is later deposited from diffusing into the underlying and adjacent dielectric layer. It is respectfully submitted that Hussein, et al. does not disclose, nor would have suggested, any equivalency of the problem of copper diffusion into silicon and into a dielectric layer, or equivalent solutions, and would not by itself or with the teachings of the IBM Technical Disclosure Bulletin article have provided any motivation for combining the teachings of Hussein, et al. and of the IBM Technical Disclosure Bulletin article. It is again emphasized that the IBM Technical Disclosure Bulletin article is only concerned with a barrier to copper diffusion into silicon, not into a dielectric film.

Attention is also respectfully directed to column 1, lines 55-57; and column 3, lines 9-13 and 58-60, of Hussein, et al. Such disclosures refer to diffusion of copper into the underlying and adjacent dielectric layer. Clearly, and contrary to the interpretation of Hussein, et al. by the Examiner, this document is concerned only with copper diffusion into a dielectric layer; and provides no basis for motivation of

utilizing, e.g., ruthenium for the neighboring film between the copper film (interconnect) and dielectric film, as in the present claims 3, 30 and 36.

The further contention by the Examiner that the IBM Technical Disclosure Bulletin article teaches that, inter alia, ruthenium is an excellent barrier against the diffusion of copper, is noted. It is respectfully submitted that this article discloses various materials, including ruthenium, as barriers against the diffusion of copper into silicon; it is respectfully submitted that this article provides no disclosure as to the use of the listed materials as a barrier against diffusion of copper into a dielectric film.

The contention by the Examiner that formation of the copper layer/neighboring film sputtering, plating, PVD and/or CVD are process limitations, and the patentability of the product must not depend on this process of production, is respectfully traversed. That is, as stated in In re Luck, 177 USPQ 523, 525 (CCPA 1973), where the processing recited provides different structure, the processing must be considered in determining patentability of the claimed structure. Applicants respectfully submit that the processing as in the present claims forms different structure in terms of, for example, roughness of the layer formed, when formed by physical vapor deposition processes such as sputtering, as compared with, for example, electroplating. In this regard, attention is directed to the enclosed Sketch, showing scanning electron microphotographs of layer structures, wherein the layers are formed by different processes such as sputtering or electroplating. Microphotographs (1)-(4) are laminated layers formed on an SiO_2 insulator; while microphotographs (5)-(8) are of layers formed on a silicon substrate. As seen on the enclosed Sketch, surface roughness increases in a specified order, with the

roughest structures being (4) and (8), wherein each of the deposited layers are formed by electroplating. Moreover, in, e.g., the structure formed in (8), the particles of copper formed are big, and electromigration is disadvantageously large. This Sketch will be submitted shortly as part of a Declaration, for supporting arguments by Applicants that the structure according to present invention is different than, for example, structure wherein each of the layers is provided by electroplating. Moreover, advantages of the structure according to the present invention is clear, from Applicants' specification as a whole. It is respectfully submitted that these microphotographs clearly show distinction between the presently claimed structure as compared with the prior art wherein, for example, all layers can be formed by electroplating; and particularly in view of advantages according to the present invention as described in Applicants' specification, clearly show patentability of the presently claimed structure made by the recited processing, over the teachings of the prior art.

As to the advantages, it is also to be noted that according to the present invention, in providing the copper or, e.g., ruthenium layer by sputtering, adherence to the underlying structure is improved because the sputtered material penetrates into the underlying layer/substrate. Particularly in view of this additional advantage achieved according to the structure of the present invention, it is respectfully submitted that the combined teachings of Hussein, et al and the IBM Technical Disclosure Bulletin article which have neither taught nor would have suggested the presently claimed structure, including the layer formed by physical vapor deposition (for example, sputtering).

The contention by the Examiner in the last three lines on page 4 of the Office Action mailed March 18, 2002, that the barrier layer (5) of Hussein, et al does prevent diffusion of copper from the interconnects (7, 30) to the bottom (22) of the via (4) into the underlying typically silicon semiconductor substrate (1) is noted. The Examiner is respectfully challenged to point out the specific portion of Hussein, et al that describes the barrier layer as preventing diffusion of copper into the underlying typically silicon semiconductor substrate. In this regard, it is emphasized that Hussein, et al, in both, column 1, lines 55-60 and column 3, lines 7-11, refers to the barrier layer 5 preventing a metal line 11 that is later deposited in each via 4, from diffusing into the underlying and adjacent dielectric layer 3 (not layers, the sole layer being described as a dielectric layer). Particularly in column 3 of this patent, there is a subsequent disclosure that diffusion of the metal into the dielectric layer 3 may cause defects in the fabricated integrated circuit. Note column 3, lines 11-13 of Hussein, et al. It is respectfully submitted that there is no basis in Hussein, et al. for the conclusion by the Examiner that the barrier layer of Hussein, et al. prevents diffusion into the underlying "typically silicon semiconductor" substrate, where Hussein, et al only refers to an underlying and adjacent dielectric layer.

Additional contentions by the Examiner in the first paragraph on page 5 of the Office Action mailed March 18, 2002, are noted. It is respectfully submitted that the Examiner has misinterpreted the teachings of the IBM Technical Disclosure Bulletin article; and has based a conclusion of motivation on this misinterpretation. Specifically, the Examiner contends that the article discloses various metals as "an excellent barrier against the diffusion of copper". However, it is respectfully submitted that this article is narrower in its teachings, describing the various metals

as an excellent barrier against the diffusion of copper into silicon. Properly interpreted, it is respectfully submitted that the IBM Technical Disclosure Bulletin article, either alone or in combination with the teachings of Hussein, et al., would have provided no motivation to combine the teachings of these references, Hussein, et al. being directed to a barrier for the underlying and adjacent dielectric layer, with the IBM Technical Disclosure Bulletin article providing a barrier against diffusion of copper into silicon.

Moreover, it is noted that present claim 3 recites a multilayered structure of the copper film interconnect, of a copper film formed through sputtering and a copper film formed through plating or chemical vapor deposition. It is respectfully submitted that the applied references would have neither disclosed nor would have suggested the multiple layers of copper, formed by the recited processing, of the interconnect, as in claim 3, and advantages thereof as described in Applicants' specification.

Again, Applicants note the Declaration to be filed shortly, including the scanning electron microphotographs attached hereto as a Sketch. If this Declaration is not in the file of the above-identified application at the time the Examiner takes up the above-identified application for consideration, it is respectfully requested that the Examiner contact the undersigned to determine the status of such Declaration. The Examiner is thanked in advance for cooperating with this request.

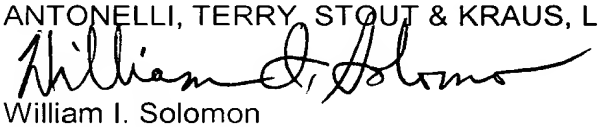
In view of the foregoing comments and amendment, and in light of the enclosed Sketch, to be incorporated in a Declaration as mentioned previously, entry of the present amendment and evidence, and reconsideration and allowance of all claims in the application, are respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment After Final Rejection. The changes are shown on the attached page captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 501.36931X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend the claims presently in the application as follows:

30. (Twice Amended) A semiconductor device having a layered interconnection structure including a copper film formed overlying a surface of a semiconductor substrate, and having a dielectric film overlying the surface of the semiconductor substrate, wherein the layered interconnection structure includes the copper film and a neighboring film adjacent the copper film, the neighboring film containing a material selected from a group consisting of rhodium, ruthenium, iridium, osmium and platinum as the primary constituent element, at least one of (a) the copper film and (b) the neighboring film being a film made by physical vapor deposition, and wherein the dielectric film is positioned such that the neighboring film is between the[cupper] copper film and the dielectric film.